

FDB52N20

200V N-Channel MOSFET

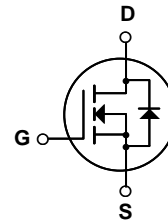
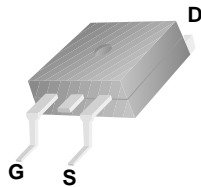
Features

- 52A, 200V, $R_{DS(on)} = 0.049\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 49 nC)
- Low C_{rss} (typical 66 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



Absolute Maximum Ratings

Symbol	Parameter	FDB52N20	Unit
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	52
		- Continuous ($T_C = 100^\circ\text{C}$)	33
I_{DM}	Drain Current - Pulsed (Note 1)	208	A
V_{GSS}	Gate-Source voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	2520	mJ
I_{AR}	Avalanche Current (Note 1)	52	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	35.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	- Derate above 25°C	357
			2.86
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB52N20	FDB52N20TM	D ² -PAK	330mm	24mm	800

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	200	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	--	0.2	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 200V, V _{GS} = 0V V _{DS} = 160V, T _C = 125°C	--	--	1 10	μA μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 26A	--	0.041	0.049	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 26A (Note 4)	--	35	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	2230	2900	pF
C _{oss}	Output Capacitance		--	540	700	pF
C _{rss}	Reverse Transfer Capacitance		--	66	100	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 100V, I _D = 52A R _G = 25Ω (Note 4, 5)	--	53	115	ns
t _r	Turn-On Rise Time		--	175	359	ns
t _{d(off)}	Turn-Off Delay Time		--	48	107	ns
t _f	Turn-Off Fall Time		--	29	68	ns
Q _g	Total Gate Charge	V _{DS} = 160V, I _D = 52A V _{GS} = 10V (Note 4, 5)	--	49	63	nC
Q _{gs}	Gate-Source Charge		--	19	--	nC
Q _{gd}	Gate-Drain Charge		--	24	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	52	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	204	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 52A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 52A di _F /dt = 100A/μs (Note 4)	--	162	--	ns
Q _{rr}	Reverse Recovery Charge		--	1.3	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 1.4mH, I_{AS} = 52A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 52A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

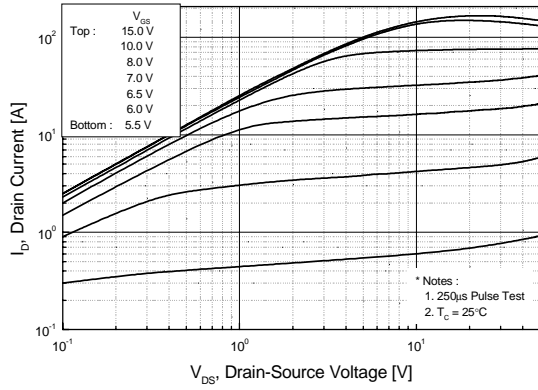


Figure 2. Transfer Characteristics

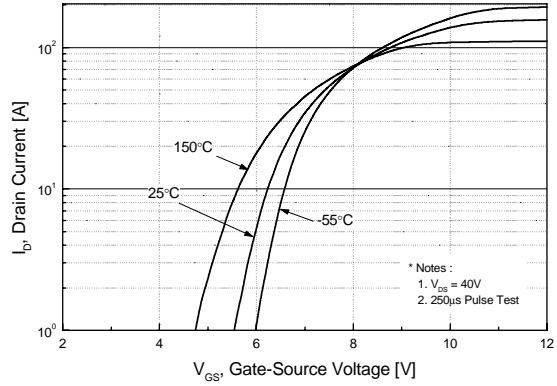


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

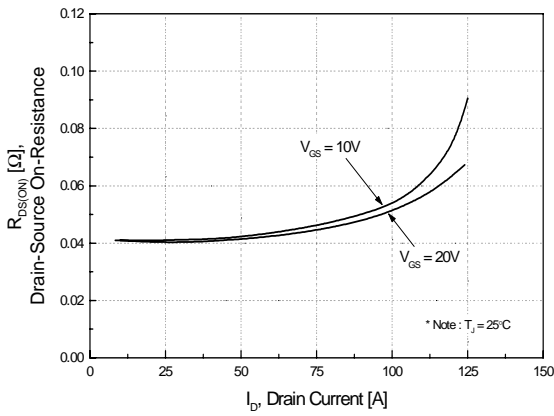


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

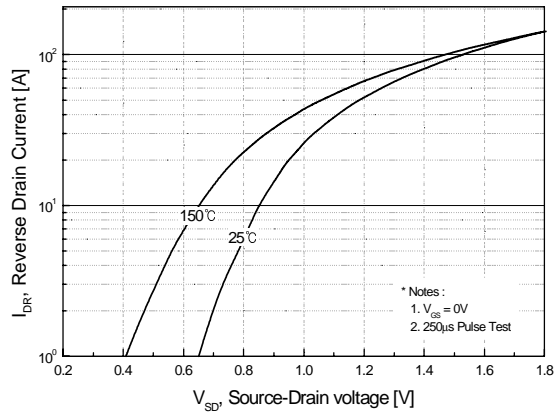


Figure 5. Capacitance Characteristics

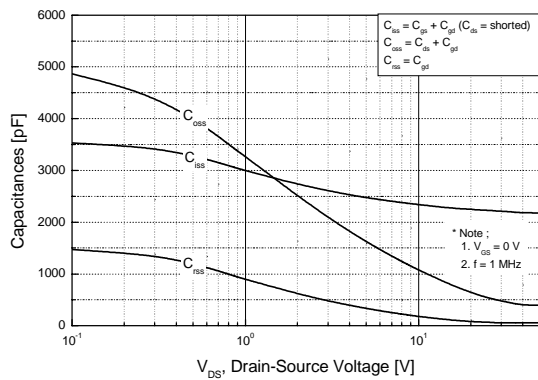
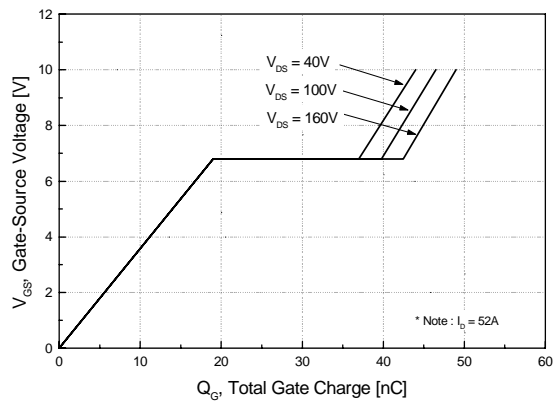


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

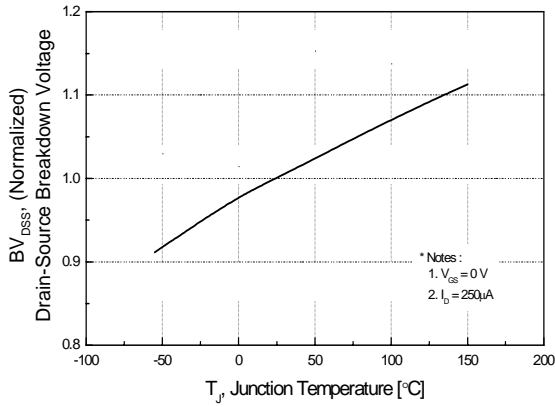


Figure 8. On-Resistance Variation vs. Temperature

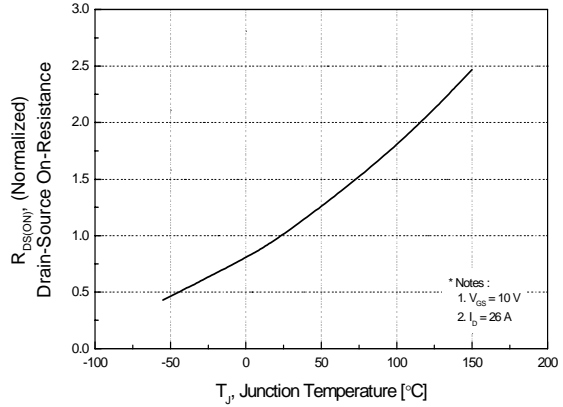


Figure 9. Maximum Safe Operating Area

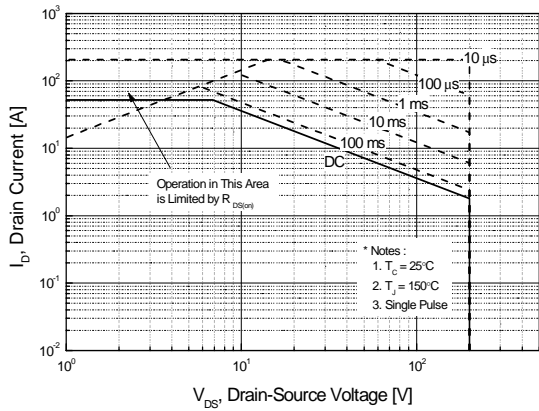


Figure 10. Maximum Drain Current vs. Case Temperature

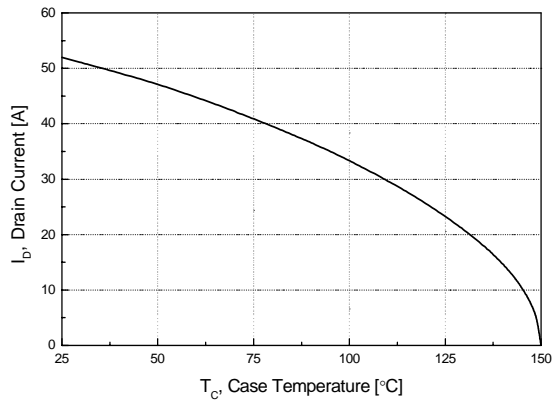
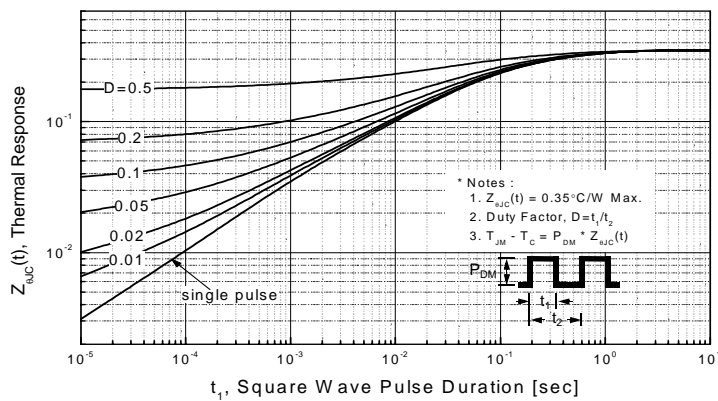
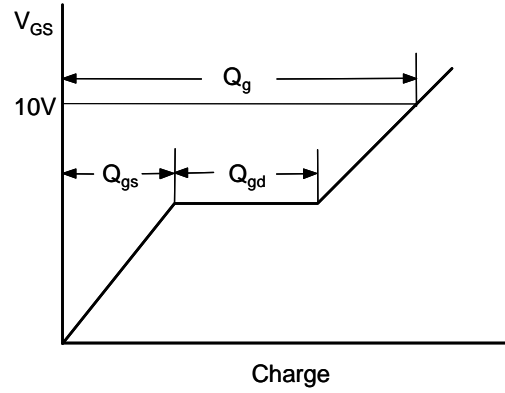
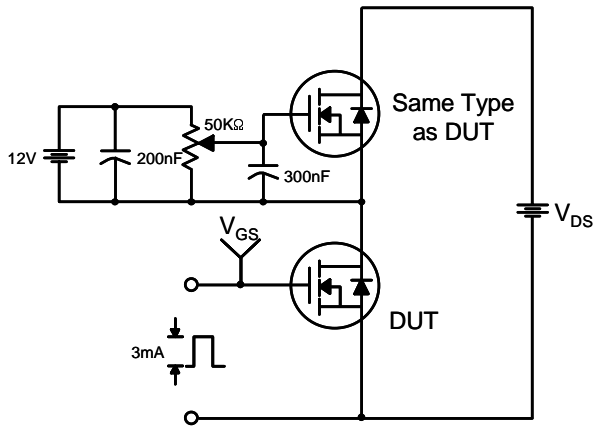


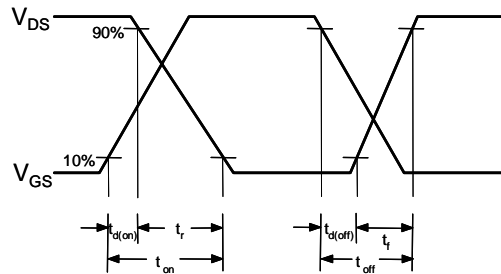
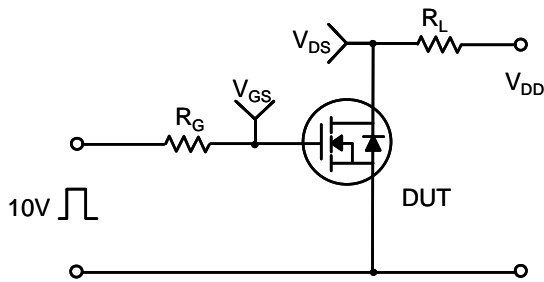
Figure 11. Transient Thermal Response Curve



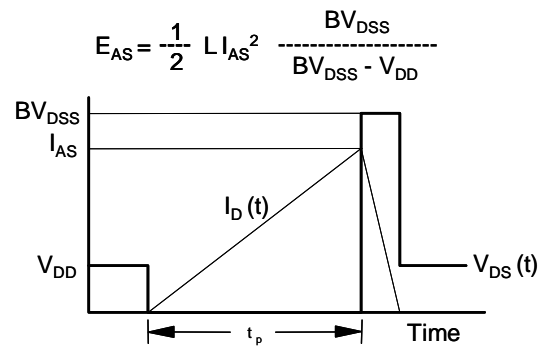
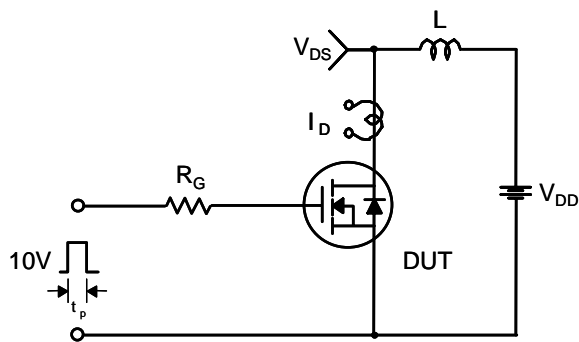
Gate Charge Test Circuit & Waveform



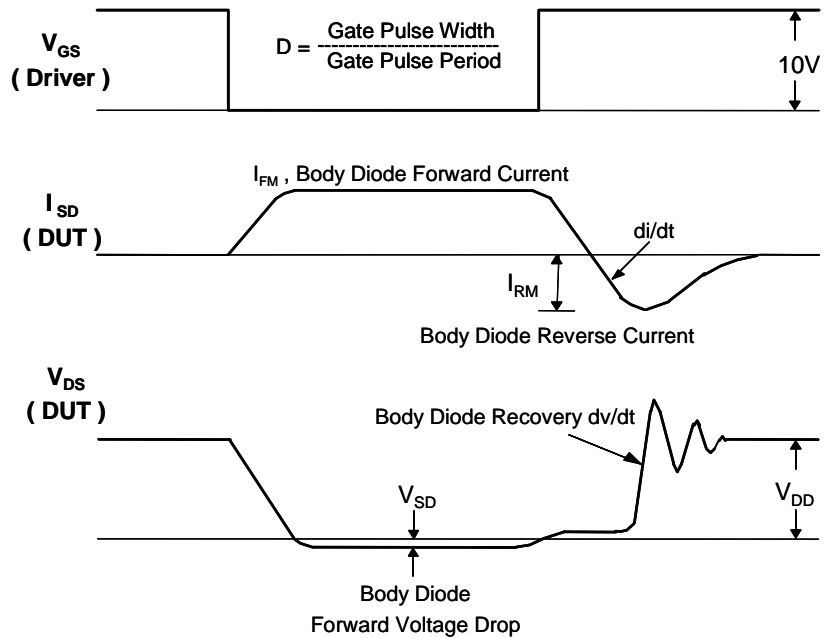
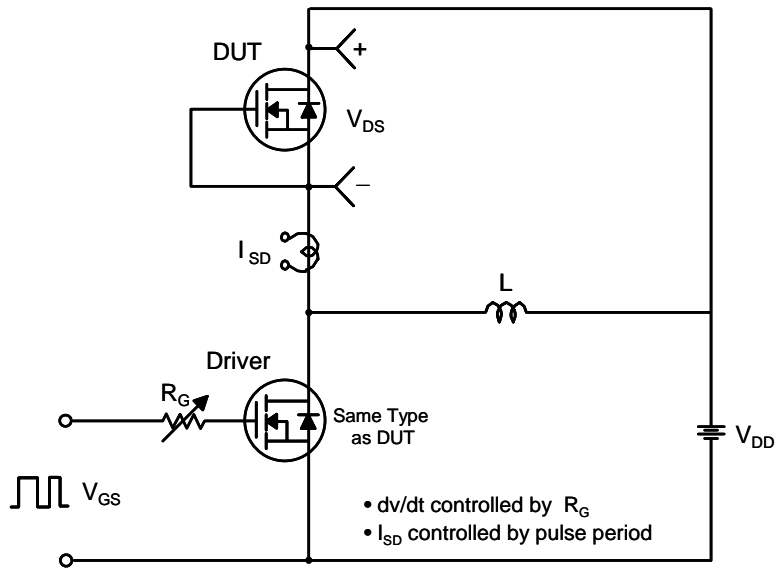
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

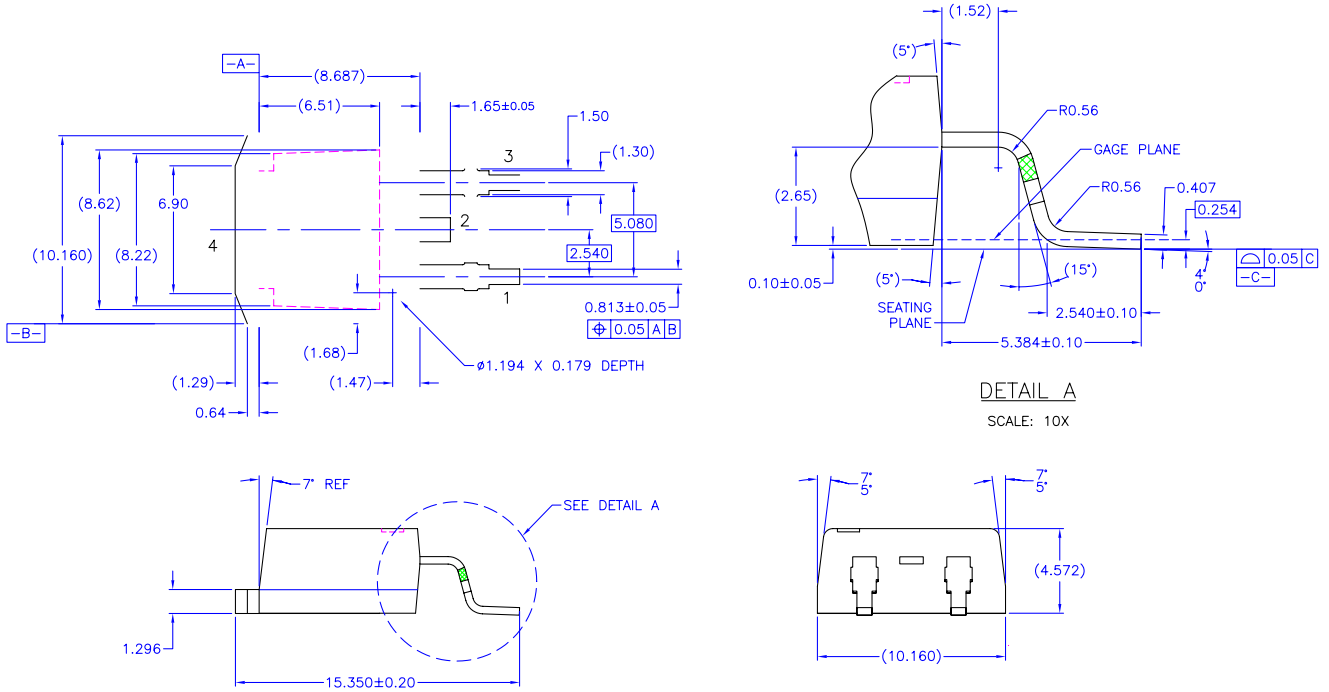


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D2-PAK








NOTES: UNLESS OTHERWISE SPECIFIED

- A) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICROMETERS MIN. 85Sn15Pb / MATTE Sn (LEAD FREE) ON LEADFRAME MATERIAL.
- B) MAXIMUM VERTICAL BURR ON LEAD TIPS NOT TO EXCEED 0.05MM FACING UP. VERTICAL LEAD TIP BURR DOWN SHOULD BE ZERO.
- C) NO PACKAGE CHIPS, CRACKS OR SURFACE INDENTATION ALLOWED AFTER FORMING.
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